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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,010	09/25/2003	Akihiro Murata	9319K-000555	4501

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EXAMINER	
LUU, CHUONG A	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,010	MURATA, AKIHIRO	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/22/2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (U.S. 6,475,896 B1) in view of Kim et al. (U.S. 6,853,433 B2).

Hashimoto discloses a semiconductor device with

(1); (7); (14; (15) forming a stress relief layer (14) on a wafer (10) such that the stress relief layer (14) is away from at least pad of electrodes (12) formed on the wafer (10);

forming a wiring layer (16) in which lines that extend from the electrodes (12) to the stress relief layer (14) are formed (see Figure 2A);

forming outer electrodes (24) that are over the stress relief layer (14) and are connected to the lines in the wiring layer (16);

forming a dielectric layer (22), where the outer electrodes are connected to form a capacitor, after the step of forming the wiring layer (see Figure 2E);

(2) forming a protective film on the wiring layer, after the step of forming the wiring layer;

forming an opening in at least part of the protective film, corresponding to the outer electrodes, before the step of forming the outer electrodes (see Figures 2D-2E);

(5) wherein, in the step of forming the dielectric layer, controlling the number of times the dielectric liquid is discharged with a discharge head for applying the dielectric liquid by the inkjet method to control the thickness of the dielectric layer forms a capacitor having a desired capacitance (see Figures 2D-2E);

(6) the method further comprising the step of forming multiple wiring layers in which stress relief layers and wiring layers are alternately deposited, adjacent wiring layers are electrically connected to each other, and the lines on the top wiring layer are connected to the outer electrodes, the step being conducted after the step of forming the wiring layer,

wherein, in the step of forming the multiple wiring layers, forming the dielectric layer between the wiring layers at portions where the adjacent wiring layers are electrically connected to each other or between the top wiring layer and the outer electrodes in the multiple wiring layers forms the capacitor (see Figures 2D-2E);

(8) forming a protective film on the wiring layer, after the step of forming the wiring layer;

forming a spiral open pattern corresponding to the inductor on the protective film, before the step of forming the inductor (see column 10, lines 4-9. Figures 2D-2E);

(9) further comprising the step of roughening the surface of the stress relief layer in a spiral pattern before the step of forming the inductor, wherein, in the step of forming the inductor, to the spiral pattern where the surface of the stress relief layer is roughened forms the inductor (see column 10, lines 4-9. Figures 2D-2E);

(10) wherein the step of roughening the surface of the stress relief layer is conducted by laser abrasion (see column 15, lines 21-23);

(13) the method further comprising the step of forming multiple wiring layers in which stress relief layers and wiring layers are alternately deposited, adjacent wiring layers are electrically connected to each other, and the lines on the top wiring layer are connected to the outer electrodes, the step being conducted after the step of forming the wiring layer, wherein, in the step of forming the multiple wiring layers, the spiral pattern forms at least one wiring layer in the multiple wiring layers to form the inductor (see Figures 2D-2E);

(16) a semiconductor device manufactured by the methods according to claim 1 (see Figures 2D-2E).

Hashimoto teaches the above outlined features except for forming a dielectric layer by applying dielectric liquid by an inkjet method. However, Black discloses a liquid crystal display with **(1); (2); (7); (9); (11); (12); (13); (14); (15)....** forming a

dielectric layer by applying dielectric liquid by an inkjet method to portions in the lines (see column 6, lines 48-53); **(3)** the method further comprising the step of sintering the dielectric layer after the step of forming the dielectric layer (see column 4, lines 5-8); **(4)** the method further comprising the steps of sintering the dielectric layer; forming a conductive layer by applying conductive liquid by the inkjet method to the sintered dielectric layer, the steps being conducted after the step of forming the dielectric layer (see column 6, lines 48-53; column 4, lines 5-8); **(11)** wherein, in the step of forming the inductor, controlling the number of times the conductive liquid is discharged with a discharge head for applying the conductive liquid to control the thickness of the conductive layer forms the inductor having a desired resistance; **(12)** wherein, in the step of forming the inductor, controlling the operation of a discharge head for applying the conductive liquid to control the number of turns in the spiral pattern forms the inductor having a desired inductance. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Hashimoto (in accordance with the teaching of Kim). Doing so would facilitate the manufacture of the semiconductor device and improve the speed of the semiconductor layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
September 6, 2005